## CLAIMS

What is claimed is:

1. A method for providing a semiconductor memory device including a substrate and at least one field isolation region, the method comprising the steps of:

(a) providing a plurality of gate stacks above the substrate, each of the plurality of gate stacks including a first edge and a second edge, each of the plurality of gate stacks crossing the at least one field isolation region;

(b) providing a source implant adjacent to the first edge of each of the plurality of gate stacks;

(c) driving the source implant under the first edge of each of the plurality of gate stacks; and

(d) providing a drain implant after the driving step (c), the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks.

2. The method of claim 1 wherein drain implant providing step (d) further includes the step of:

(d1) providing a second source implant and the drain implant after the driving step (c) the second source implant being provided in the substrate adjacent to the first edge of each of the plurality of gate stacks and the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks.

3. The method of claim 1 wherein source implant providing step (b) further

includes the step of:

(b1) providing a first source implant and a second source implant adjacent to the first edge of each of the plurality of gate stacks; and wherein driving step (c) further includes the steps of:

(c1) driving the first source implant and the second source implant under the first edge of each of the plurality of gate stacks.

4. The method of claim 1 further comprising the step of:

(e) providing a first spacer and a second spacer for each of the plurality of gate stacks, the first spacer being disposed along the first edge of each of the plurality of gate stacks, the second spacer being disposed along the second edge of each of the plurality of gate stacks.

5. The method of claim 4 further comprising the step of:

(f) providing a self-aligned source etch.

6. The method of claim 4 wherein the semiconductor memory device further includes a periphery including a plurality of logic devices and wherein the spacer providing step (e) further includes the step of:

(e1) providing the first spacer and the second spacer concurrently with a plurality of spacers in the periphery of the semiconductor memory device.

7. The method of claim 1 wherein the drain implant is As.

8. The method of claim 5 wherein the second source implant is As.

9. The method of claim 1 further comprising the step of:

(e) providing a rapid thermal anneal after the drain implant has been provided.

10. A semiconductor memory device including a substrate, the semiconductor device comprising:

a plurality of gate stacks above the substrate, each of the plurality of gate stacks having a first edge and a second edge;

at least one source for each of the plurality of gate stacks, each of the at least one source including a source implant, the source implant being provided in the substrate adjacent to the first edge of each of the plurality of gate stacks and driven under the first edge of each of the plurality of gate stacks prior to the first spacer and second spacer being provided;

at least one drain for each of the plurality of gate stacks, the at least one drain including a drain implant, the drain implant being provided in the substrate adjacent to the second edge of each of the plurality of gate stacks, the drain implant being provided after the at least one source implant is driven under the first edge of each of the plurality of gate stacks.

11. The semiconductor device of claim 10 wherein the source implant includes a first source implant, the first source implant being provided in the substrate adjacent to the first edge of each of the plurality of gate stacks and driven under the first edge of each of the

plurality of gate stacks prior to the drain implant being provided;

and wherein the at least one source further includes a second source implant being provided after the first spacer and second spacer are provided, the second source implant further being provided in the substrate adjacent to the first spacer.

12. The semiconductor device of claim 10 wherein the source implant includes a first source implant and a second source implant, the first source implant and second source implant being provided in the substrate adjacent to the first edge of each of the plurality of gate stacks and driven under the first edge of each of the plurality of gate stacks prior to the drain implant being provided.

13. The semiconductor device of claim 10 further comprising:

a first spacer and a second spacer for each of the plurality of gate stacks, the first spacer being disposed along the first edge of each of the plurality of gate stacks, the second spacer being disposed along the second edge of each of the plurality of gate stacks.

14. The semiconductor memory device of claim 13 further including a periphery including a plurality of logic devices and wherein the first spacer and the second spacer are provided concurrently with a plurality of spacers in the periphery of the semiconductor memory device.

15. The semiconductor memory device of claim 10 wherein the drain implant is As.

16. The semiconductor memory device of claim 15 wherein the second source implant is As.